

FIG. 1 (PRIOR ART)



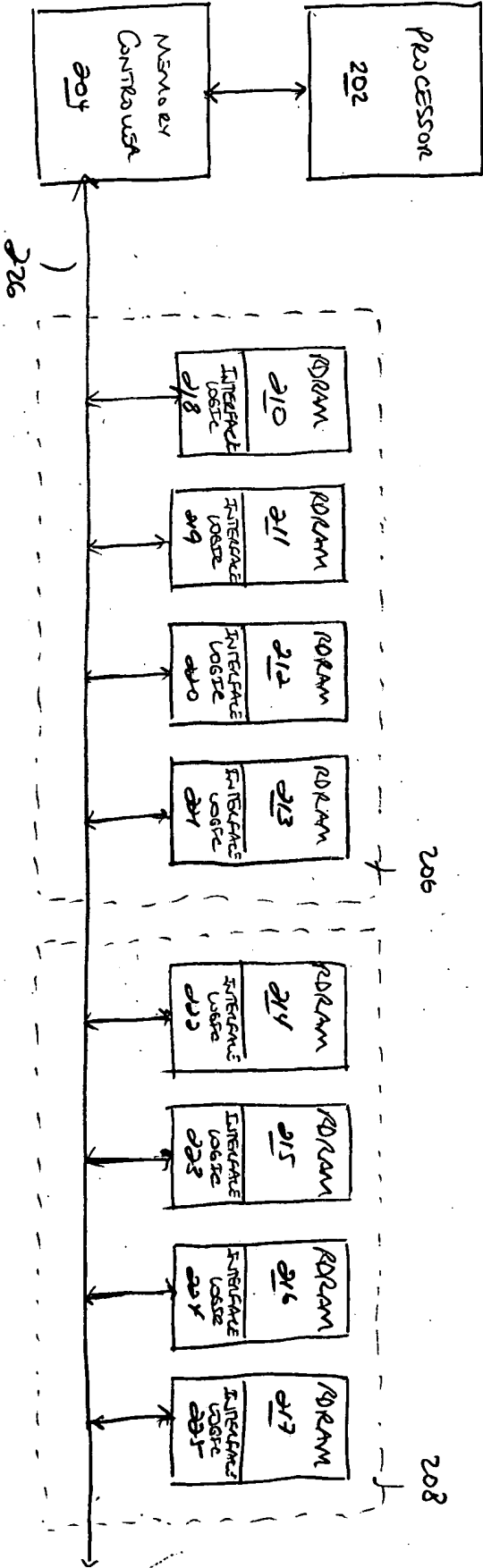
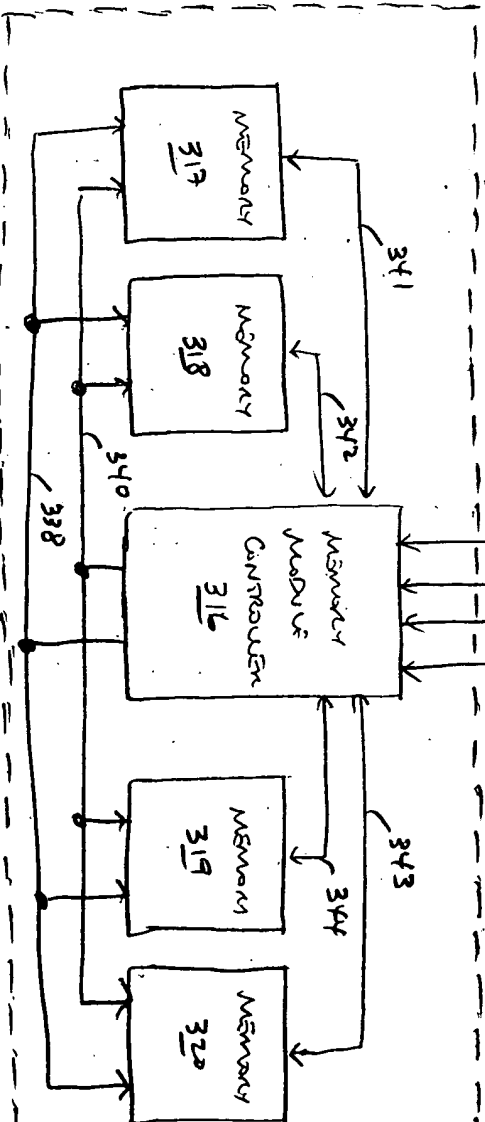
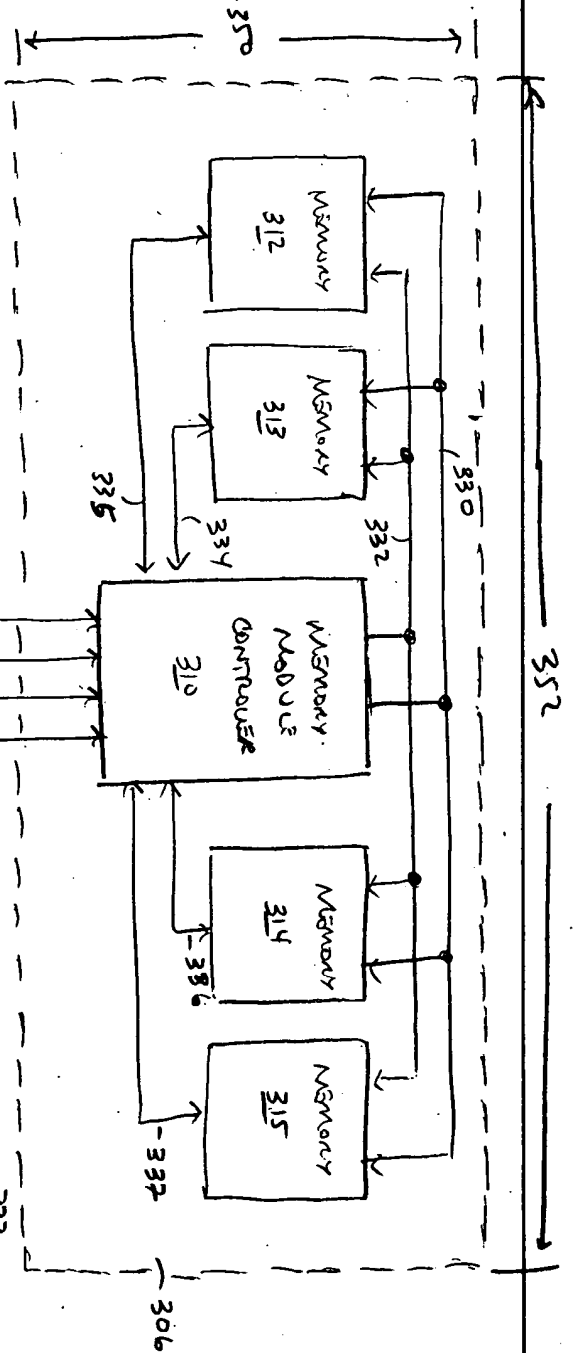
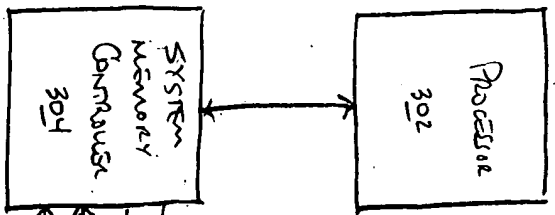


FIG. 2 (Prior Art)



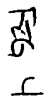
22-141 50 SHEETS  
22-142 100 SHEETS  
22-144 200 SHEETS



SYSTEM MEMORY BUS 323

FIG. 3





- 500

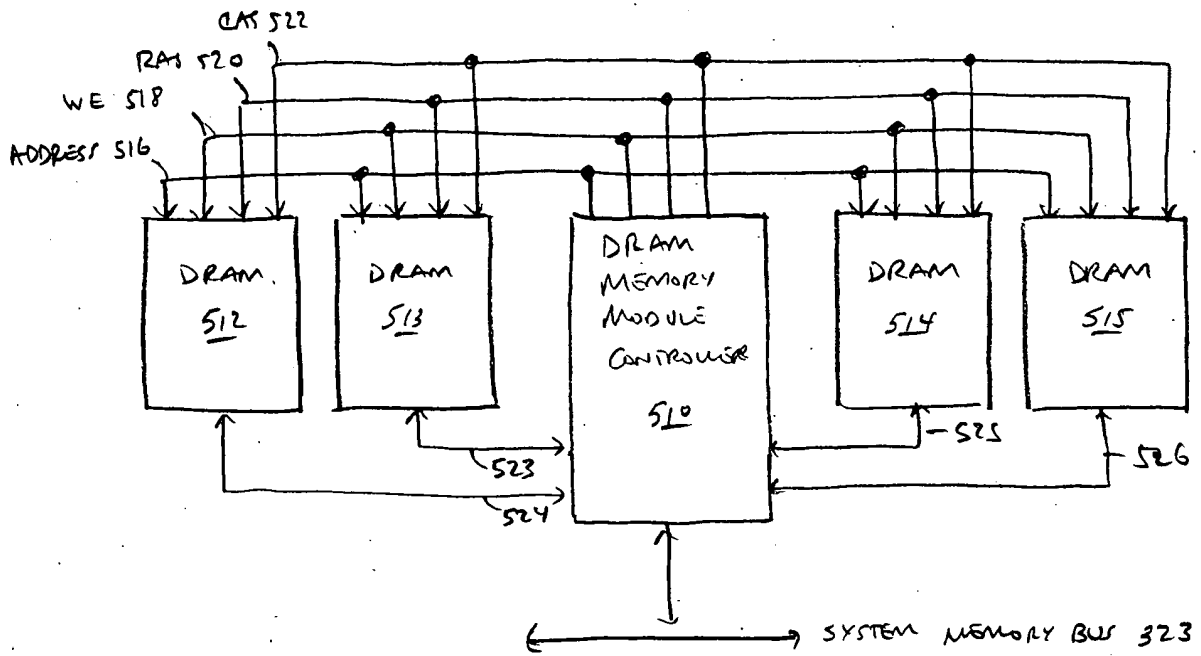


FIG. 5

- 600

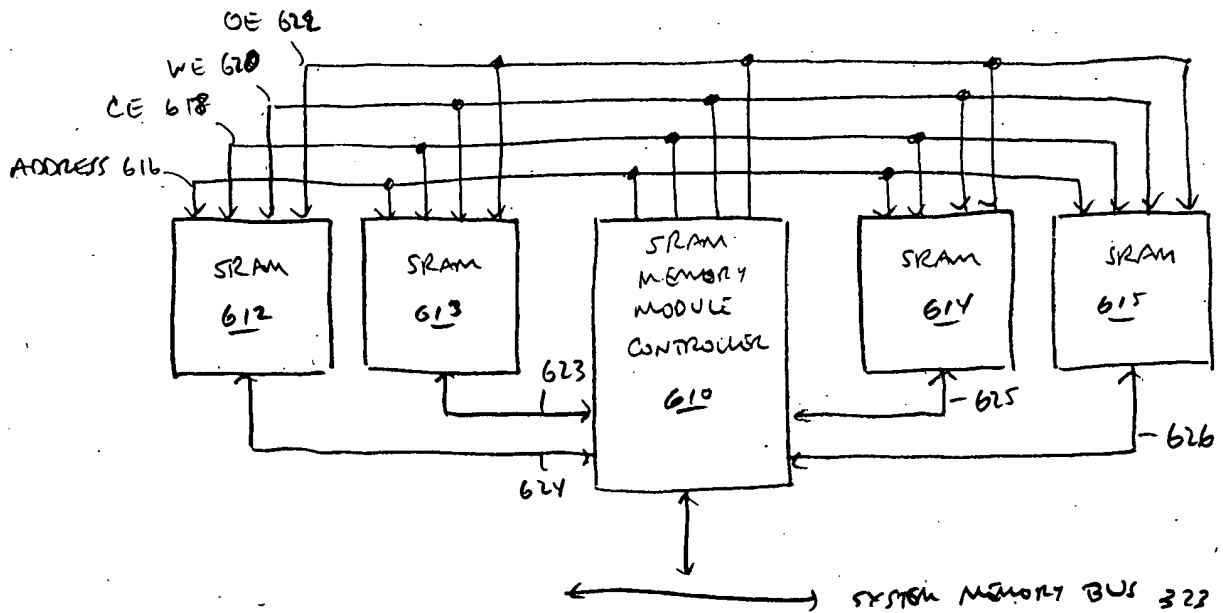


FIG. 6



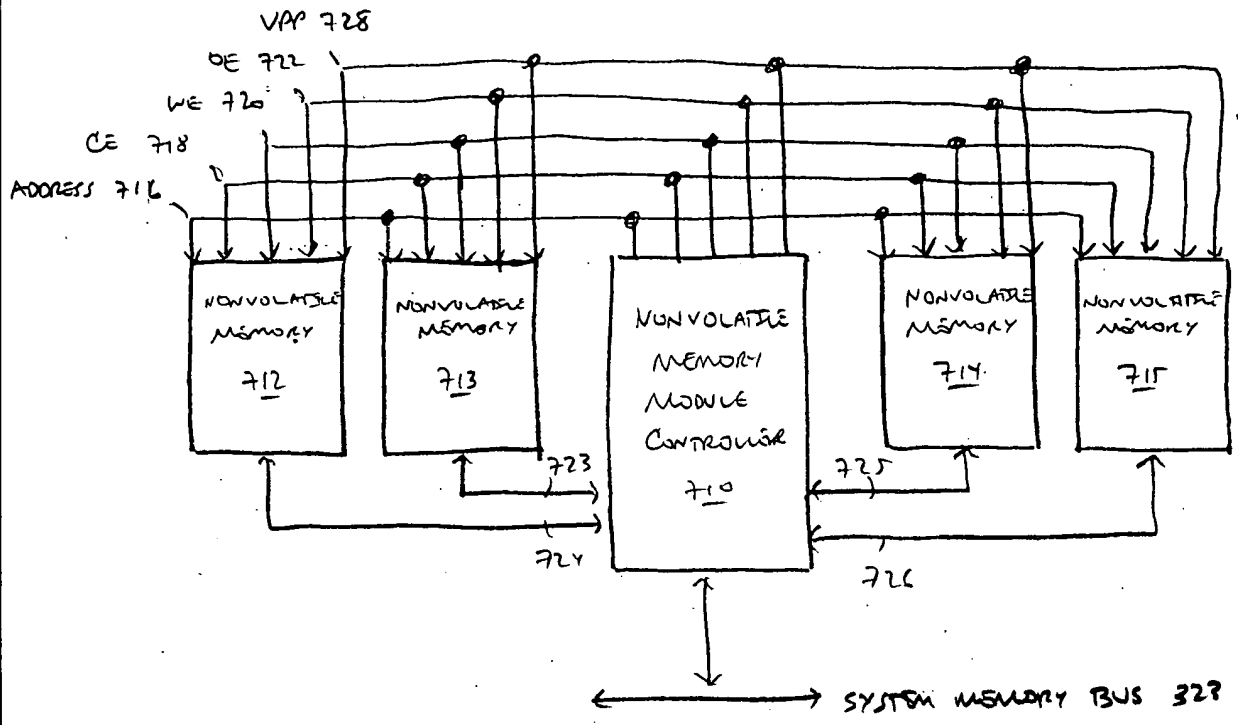


FIG. 7



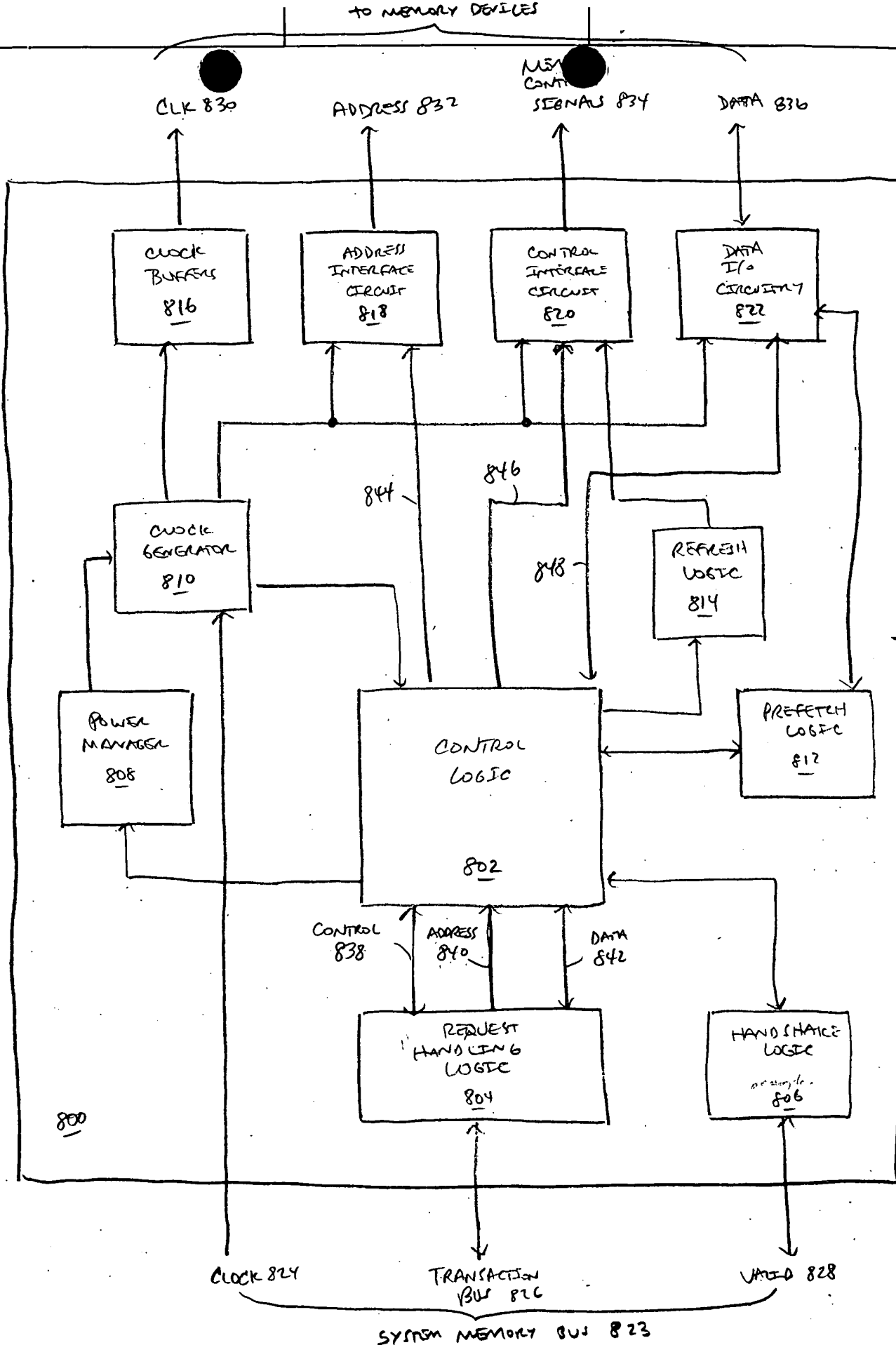


FIG. 8



SECRET

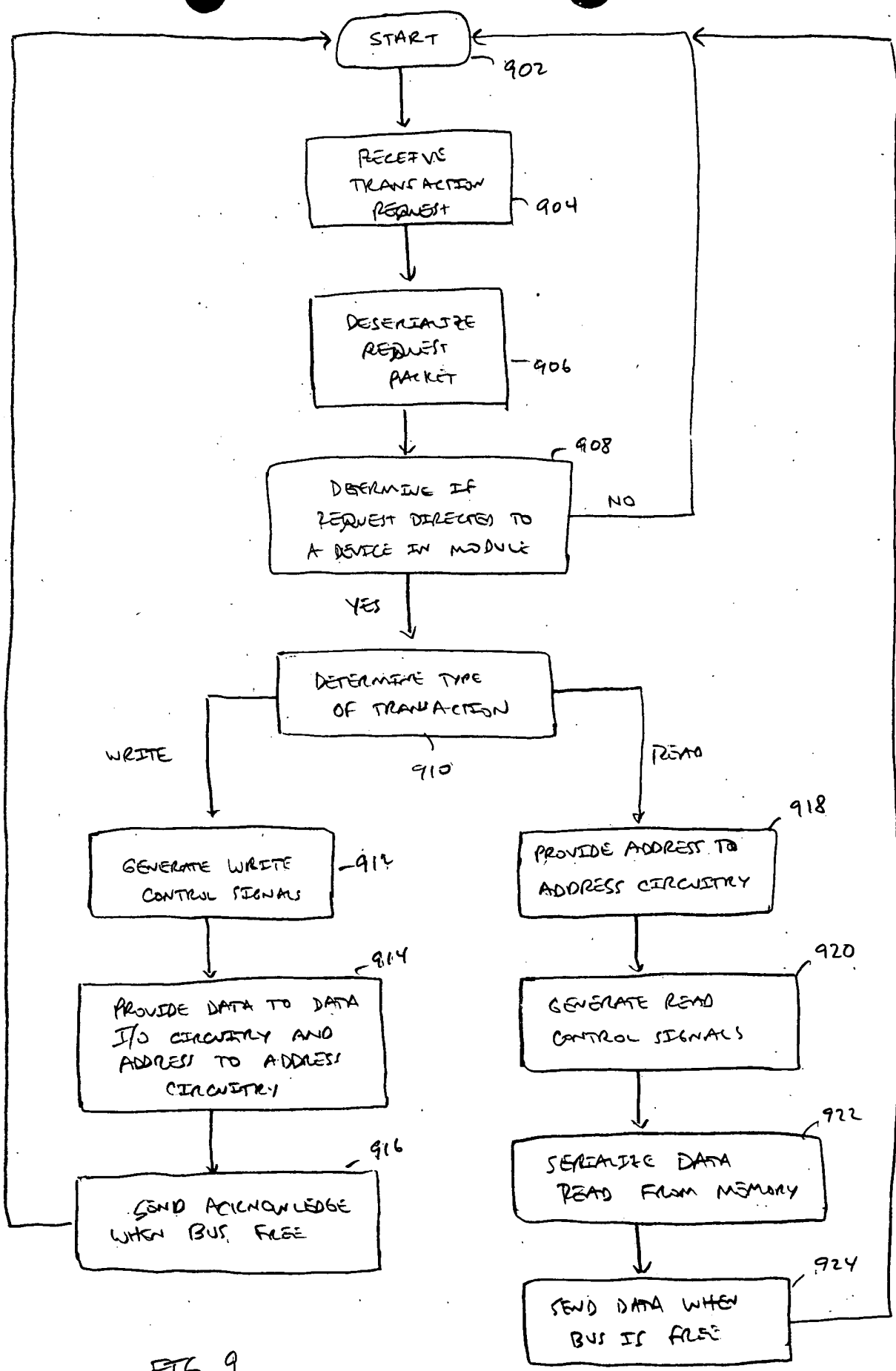
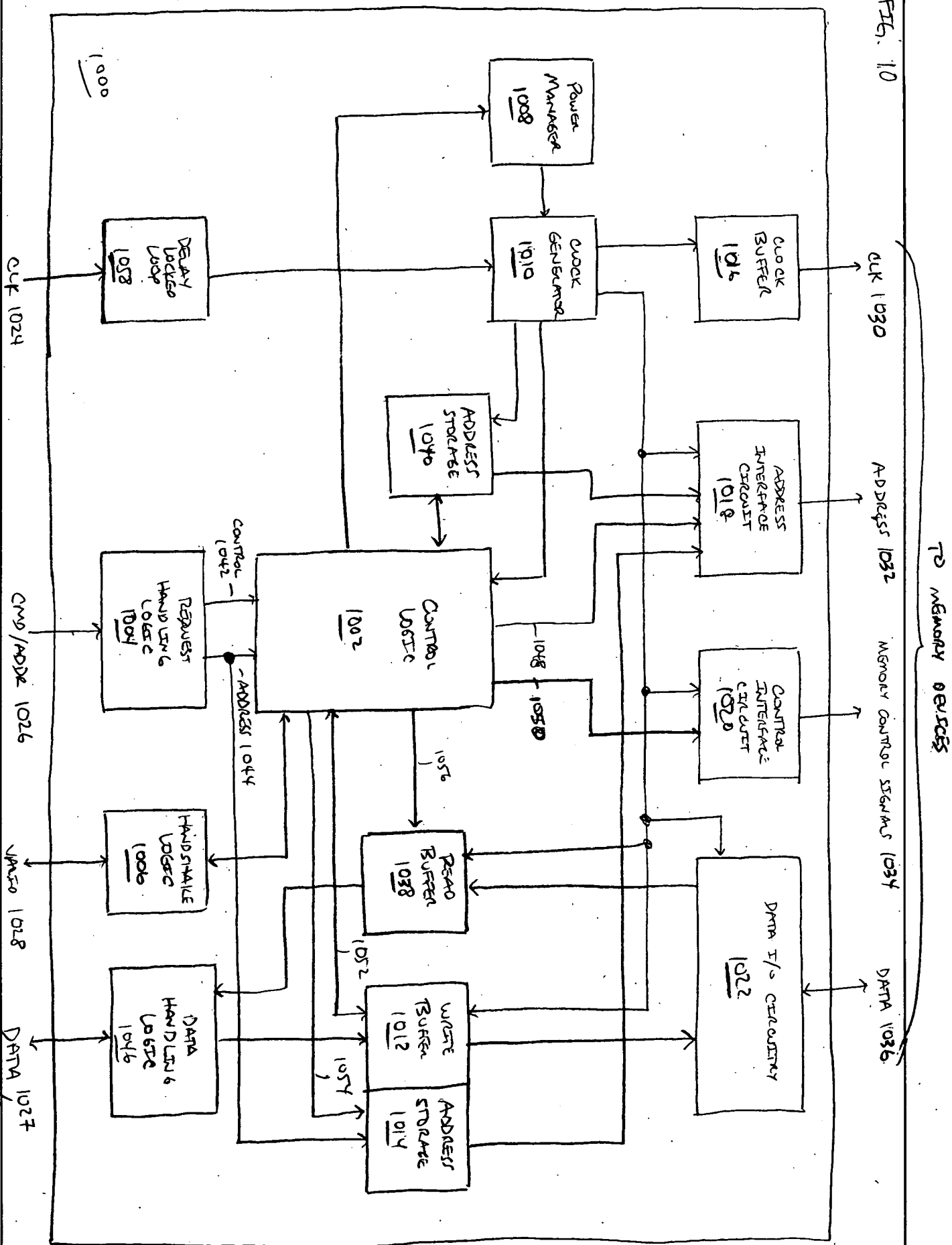


FIG. 9



FIG. 10



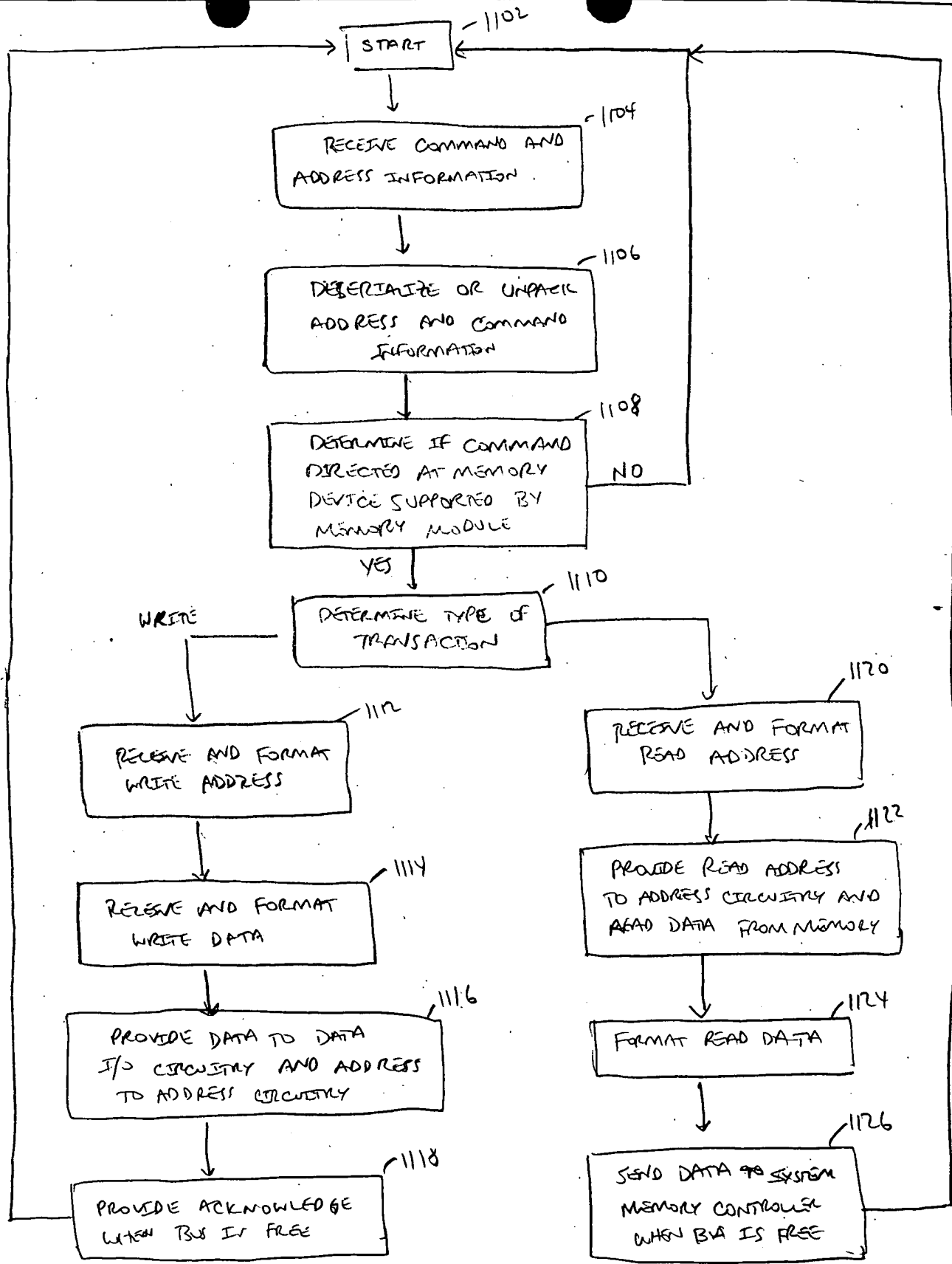


FIG. 11

1200

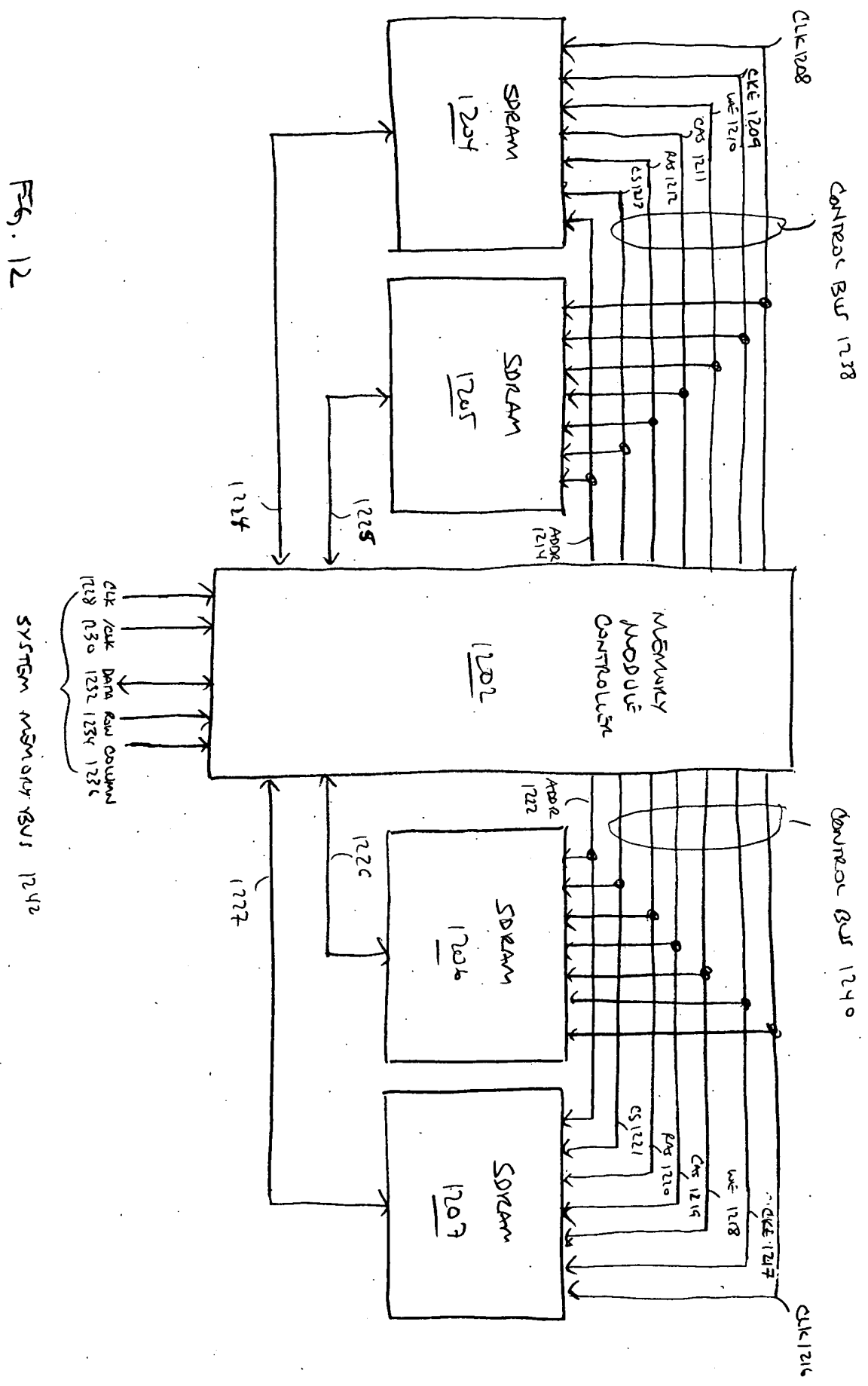


Fig. 12



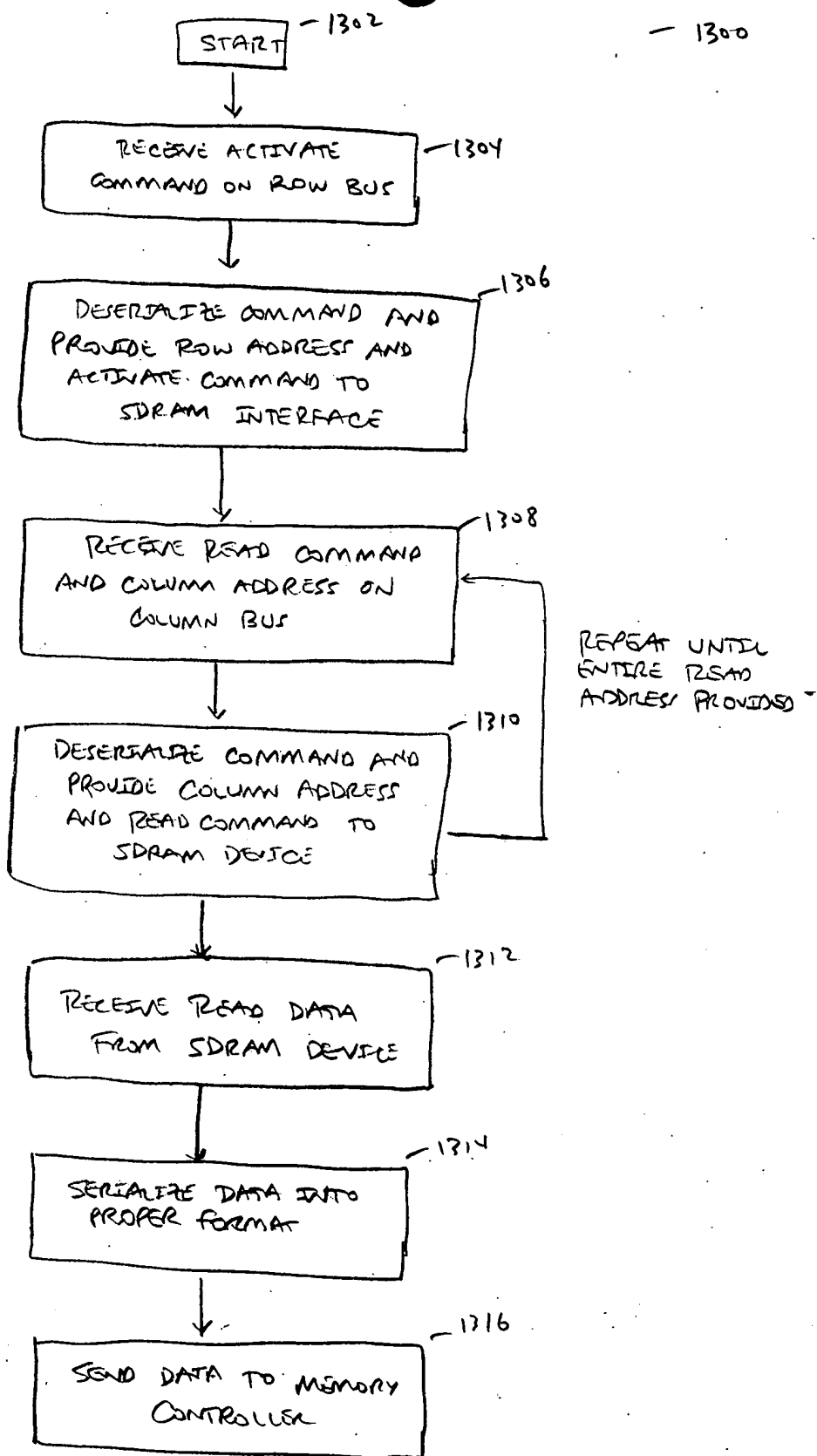


Fig. 13

CLK 1228



Row 1234



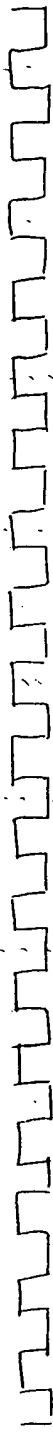
Column 1236



Data 1232



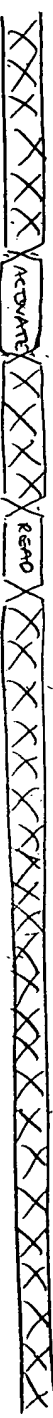
CLK 1208, 1216



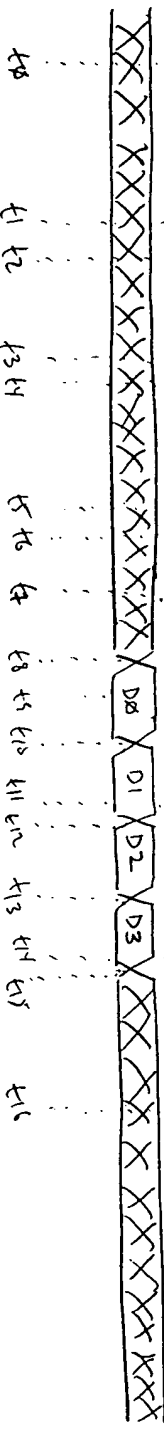
ADDR 1214, 1222



Control Bus 1238, 1240



Data 1224-1227



FS6 14



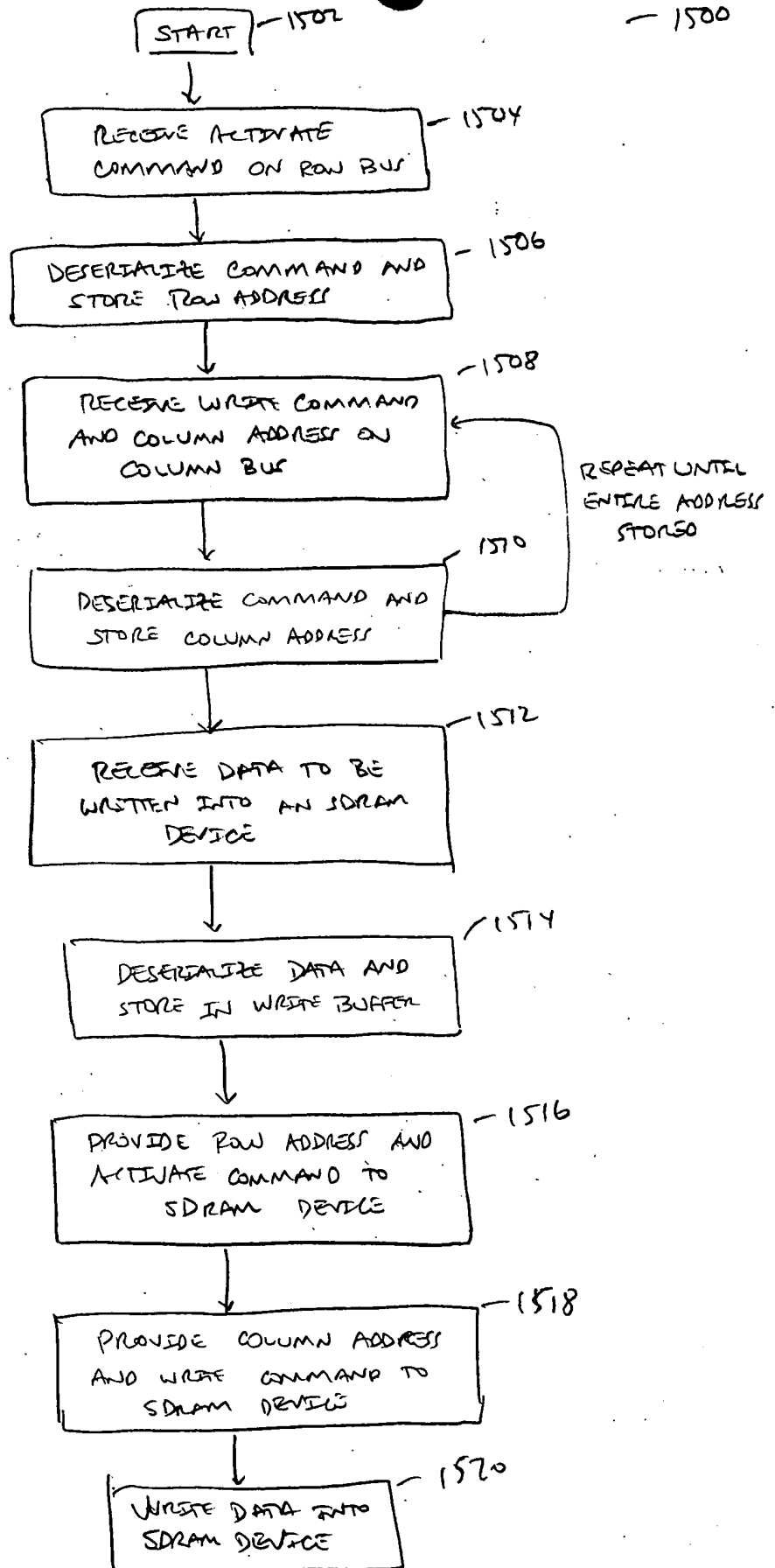
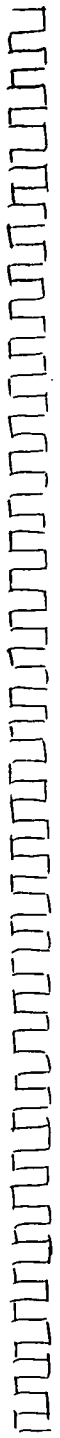


FIG. 15

die 1228



Row 1234



Column 1236



DATA 1232



Clock 1208, 1216



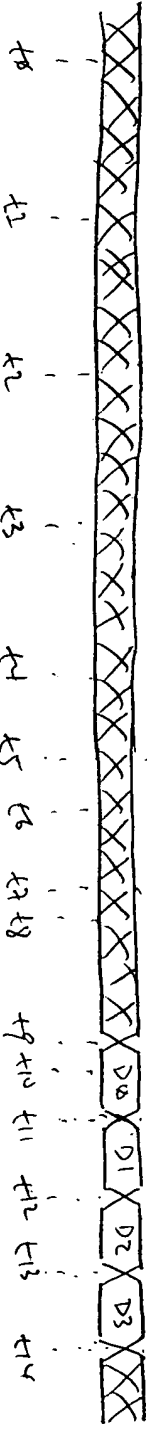
ADDR 1214,  
1222



Control  
BUS 1238, 1240



DATA 1224-  
1227

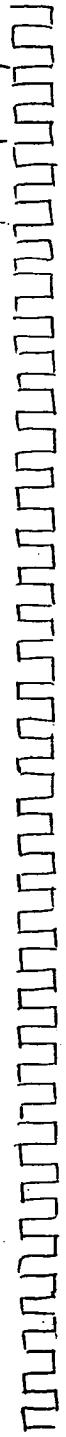


t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14

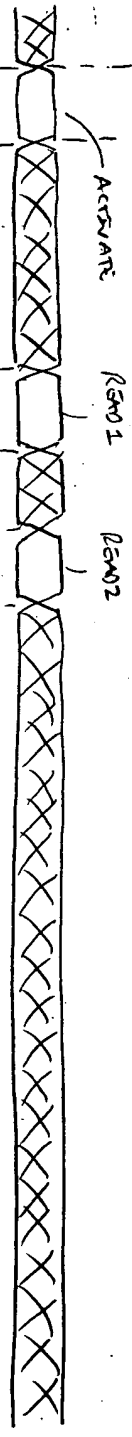
Fig. 16



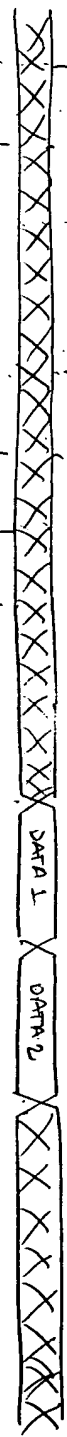
Clock 1228



CONTROL BUS 1235



DATA 1232



Clock 1208, 1216



ADDR 1214, 1222



CONTROL BUS 1238, 1240



DATA 1224-1227



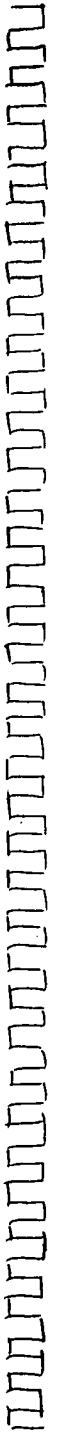
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16 t17

Fig. 17





CLK 1228



ACTIVE

WRITE 1

WRITE 2

CONTROL BUS 1235



DATA 1232



CLK 1208, 1216



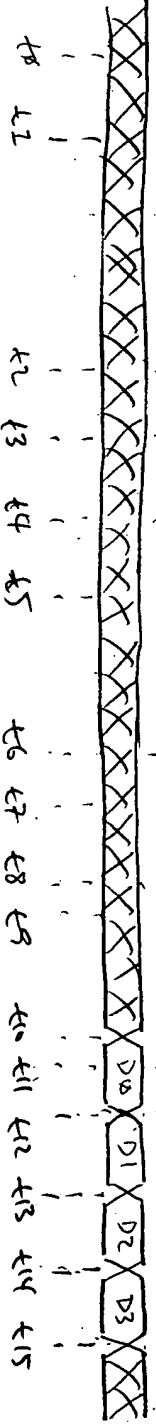
ADDR 1214, 1222



CONTROL BUS 1238, 1240



DATA 1224-1227



t0 t1

t2 t3 t4 t5

t6 t7 t8 t9

t10 t11 t12 t13 t14 t15

FIG. 18

